Multi-function radar systems for the deployed warrior using VPX-REDI and RapidIO

By James Meyer

Next-generation radar will need to provide enormous flexibility in terms of modes and functions. This application requirement will drive performance demands that have architectural implications for radar computing and electronics.

Advanced Multi-Function Radar (MFR) systems must simultaneously provide multimode search, multitarget tracking, Synthetic Aperture Radar (SAR) imaging, and Space Time Adaptive Processing (STAP). These systems will be deployed in some of the harshest and most demanding environmental conditions inside Unmanned Aerial Vehicles (UAVs), manned aircraft, and ship- and ground-based radar systems. The combined requirement of performance and ruggedization makes it challenging to service MFR applications using yesterday’s Commercial Off-the-Shelf (COTS) technologies. However, COTS solutions based on open standards are now meeting the challenge of next-generation requirements. The combination of massive fabric bandwidth, Field Programmable Gate Array (FPGA) processing power, PowerPC high-compute density farms, and standards-based I/O housed in a conduction-cooled system address the simultaneous requirements of performance within an enclosure that can face the extremely hazardous field conditions found in deployed radar. VPX-REDI, a next-generation standard that combines the VITA 46 and VITA 48 standards (www.vita.com) with RapidIO (www.rapidio.org), significantly advances the robustness and performance of COTS sensor computing.

Challenges of mission-critical systems

Figure 1 shows an example flow of front-end data acquisition to back-end data processing and control. The challenge is to engineer and integrate highly reliable mission-critical systems that provide the deployed warrior with radar and navigation capabilities required for very challenging missions.

A typical leading-edge problem involves minimizing the enemy’s broadband jamming efforts or eliminating ground or sea clutter located at arbitrary or unknown locations. The solution is to compute and track the angular locations of the jammers or clutter by appropriately processing the received signals and then adaptively generating a time-and-frequency-varying antenna pattern that places angular pattern nulls at the computed jammer location(s). Actual implementation depends upon a number of basic capabilities:
- Multielement antenna (8 to 100 elements)

- Separate receiver channel and A/D for each element/channel
- Efficient mapping of dedicated hardware for the pulse compression algorithms on FPGA modules
- Tightly coupled fabric connectivity for corner-turning operations
- Data exchanges with the high compute density processing modules for the final STAP and data processing

The I/O distribution for the STAP application described above entails more than 10 GBps of bisection bandwidth within a system and gigaflops of processing power. The two most challenging areas of the problem, shown in Figures 2 and 3, are the real-time receive beamforming computational rate at up to 40 MHz and the adaptive beam-forming weight computations at a rate of 100 Hz to 1,000 Hz.

Open standard COTS systems
By providing a modular COTS system based on open standards, the exceptionally demanding I/O in GBps and processing requirements of 10 to 100 GFLOPS for STAP and SAR algorithms can be met by combining the front-end functionality of high-speed microwave tuners and high-speed A/Ds in the speed range of 3 GHz or greater. Additionally, FPGAs and PowerPC resource modules are used for dedicated high-speed computations such as pulse compression operations for high-range resolution; effective short pulse response derived from the long, high-energy transmitted pulses; and lastly, returns. The complete processing chain operating on the three-dimensional (3D) radar data cube is shown in Figure 4.
individual electronics modules are swapped out by the end user.

New radar systems require 2 Level Maintenance (2LM) where processors, FPGAs, and RapidIO fabric technologies including standard I/O mezzanine cards, PowerPC also support for an interconnected common set of building block other form factor architectures, namely VXS (VITA 41). There is a slot be dedicated to fabric switching, as is the general case in full mesh provides all-to-all connectivity without requiring that support an expansive, full-mesh compute fabric topology through the implementation of corner-turning for the SAR algorithm at the maximum data rates of the packet switched Serial RapidIO fabric. The gold standard measure of fabric bandwidth in an all-to-all data exchange such as this one is bisection bandwidth. Bisection bandwidth measures the interconnect capacity between any randomly drawn halves of a topology. A RapidIO fabric in a dual-star configuration can exceed 16 GBps of aggregate bisection bandwidth.

Algorithm challenges
To meet the grand algorithm challenges of today and tomorrow, such as the STAP spatial processing algorithm, a modular, hardware architecture – based on a new VITA standard form factor and switched I/O fabric – is required. The focus of the future STAP-capable radar system solution described later will be implemented using the larger 6U format of the VPX-REDI standard along with the Serial RapidIO switched fabric. The new system design, based on the new VPX-REDI form factor standard (VITA 46 and 48), provides the compute power and I/O bandwidth necessary to fully implement the STAP and SAR algorithms mentioned earlier. The PowerStream 6600 VPX-REDI rugged computer system from Mercury Computer Systems is an example of such a system. It can achieve more than 34 GBps of system-wide RapidIO fabric throughput. Its 16 modules can house 64 PowerPC processors or alternatively 21 user-programmable Xilinx Virtex-4 FPGAs. All this is accomplished in a conduction-cooled format made possible by the breakthrough VPX-REDI form factor.

The corner-turn (Figure 2) is one of the greatest challenges facing radar processing systems. VPX-REDI introduces a new module format based on a new set of high-speed differential signaling connectors. The adoption of a new connector set in the VPX-REDI standard paves the way for higher speed signaling, greater power budgets, and an enormous increase in I/O capabilities. VPX-REDI systems can achieve hundreds of GBps of system throughput using high-speed serial fabric interconnects. One key difference in the architecture of VPX-REDI is its ability to support an expansive, full-mesh compute fabric topology through an increased number of serial fabric links on each module. The full mesh provides all-to-all connectivity without requiring that a slot be dedicated to fabric switching, as is the general case in other form factor architectures, namely VXS (VITA 41). There is also support for an interconnected common set of building block technologies including standard I/O mezzanine cards, PowerPC processors, FPGAs, and RapidIO fabric.

2 Level Maintenance
New radar systems require 2 Level Maintenance (2LM) where individual electronics modules are swapped out by the end user, literally in the field, when a failure occurs. VPX-REDI provides the electrical and mechanical infrastructure that protects individual electronics modules from static discharge (ESD) when they are being handled by ungrounded service personnel. This includes specially designed backplane connectors, carefully placed GND signals to sink excess current, and robust module covers.

Ruggedization
Mobile applications impose certain constraints on computing. Ground mobile vehicles can operate in regions of extreme temperature and in locations where the air is dusty or worse: chemically contaminated. This environment precludes the use of air convection cooling. Conduction cooling provides passive means by which heat can be conducted from the card to the outside wall of the chassis. The chassis wall can be cooled with a fan, but this has none of the implied problems of blowing air directly across the board. The conduction-cooling board exoskeleton also provides reinforcement for high-shock and vibration applications.

Airborne applications tend to prefer air cooling because it is lighter in terms of weight than conduction cooling. However, tactical fighters that achieve heights of 70,000 feet may have difficulty cooling electronics at low pressure. Despite its disadvantage of weight, these types of airborne applications also choose to make use of conduction cooling.

The solution
The radar compute subsystem that addresses the above-mentioned requirements comprises a VPX-REDI chassis and three basic processing modules that are connected via a Serial RapidIO backbone fabric and other backplane interconnects. The conduction-cooled modules in the system include an I/O mezzanine carrier, a PowerPC signal processing card, and an FPGA compute resource card. The VPX-REDI backbone provides a means for each slot to transfer data to any other of 16 slots via a RapidIO fabric interface without the use of a central switch card.

The I/O carrier module is a smart (processor-based) I/O mezzanine carrier that also serves as the scalar data and control processor for the radar receiver/exciter. It contains two MPC8548 processors that can serve as application processors or I/O engines servicing respective mezzanine card sites. The two mezzanine cards support PMC-X or XMC interfaces. This provides systems integrators with a wide and established ecosystem of option cards that may be incorporated.

The High-Compute-Density (HCD) module is a quad PowerPC AltiVec processor resource board. Each MPC7448 processor on the HDC operates at 1.4 GHz with a 400 MHz DDR2 memory interface. Each HCD module contains four PowerPC Compute Nodes (CNs) connected by a low-latency RapidIO crossbar to implement the network of fully connected floating point processors necessary to provide the GFLOPS of processing power for SAR and STAP algorithms.
The FPGA resource board houses three user-programmable Xilinx Virtex-4 FPGAs and can be delivered with an FPGA Developer’s Kit (FDK). This kit puts the basic building blocks needed for system integration at the fingertips of developers: RapidIO fabric and Serial FPDP bridge end-point IP, data movement functionality, memory controllers, and so on.

A holistic solution for next-generation radar
Multi-function radar presents enormous challenges for system integrators, but COTS solutions based on open standards are now meeting them. The combination of massive fabric bandwidth, FPGA processing power, PowerPC high-compute density farms, and standards-based I/O is one important set of ingredients in challenging multi-function radar applications. The additional challenge is to house these features within a conduction-cooled enclosure that can face the extremely hazardous field conditions characteristic of field deployments.

James Meyer is a senior systems applications engineer at Mercury Computer Systems. He is responsible for applying Mercury’s high-performance multicomputer technology to customer projects including radar and sonar signal processing systems. Prior to joining Mercury, James worked at CSPI and Radix Systems on the development of noise abatement systems for submarines. He earned a Masters in Computer Science from Johns Hopkins University and a dual Bachelor’s degree in Electrical Engineering and Bioengineering with honors from Syracuse University.

To learn more, contact James at:

Mercury Computer Systems, Inc.
199 Riverneck Road
Chelmsford, MA 01824
Tel: 301-572-3012
E-mail: meyer@mc.com
Website: www.mc.com