

In the world of high-performance data acquisition and data recording, a perfect storm is brewing

System architects seek greater bandwidth and faster peripherals

By Philip Brunelle

Emerging bus architecture standards such as PCI Express and other technology advances are converging to create a new world for high-speed data capture. There's enormous opportunity for growth as PCI Express replaces shared bus architectures with its point-to-point functionality. With 30x performance improvements over base PCI implementation, we will see an impressive theoretical threshold of 4 GBps top-end performance, thus breaking down traditional barriers to high-end data acquisition and recording.

In the world of real-time systems, standard bus architectures including PCI, VME, PXI, and CompactPCI are fundamental to addressing a broad spectrum of high-performance applications with modular instruments and high-speed recording devices. Data movement within a real-time system is throttled by the slowest link in the overall architecture. While performance has been widely addressed for CPU, disk drive, RAM, and network architectures, the data bus available in standard motherboards continues to rank as the slow zone of total system throughput. But now with emerging standards like PCI Express, a new world of nearly unlimited bandwidth is quickly unfolding. The elements are converging to form the perfect storm of high-speed data capture.

In with the new, out with the slow

The PCI bus has long been the standard for expanding general purpose PCs to enable a broad range of I/O, storage, and networking capabilities. At its inception, the PCI bus provided an impressive 132 MBps performance in a 32-bit architecture. This performance, however, is only a theoretical limit. In practice, the PCI bus is designed to be shared among multiple devices. Just as traffic lights regulate the flow of interconnected roadways, a bus manager or arbitrator ensures equitable use of the PCI bus by one or more competing resources. The arbitrator, by itself, results in performance degradation and a 20-25 percent overhead. The practical limit on the 32-bit bus is therefore significantly slower, or less than 100 MBps. In fact, the device may have to share the available bandwidth with other devices on the shared PCI bus, and the result can be significantly lower than 100 MBps.

Because of the limitations of the PCI bus, designers have used serial fiber data links and specialized controllers that bypass CPU and bus limitations to achieve data recording rates in excess of 200 MBps (see Figure 1).

Over the years, chip designers have been able to compensate by developing new offerings like 64-bit and higher clock rate versions of the PCI bus. While each successive standard provides

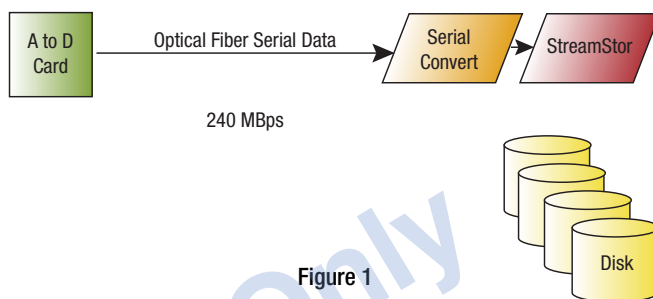


Figure 1

higher aggregate bandwidths, system architects have struggled to overcome the inherent complexities and limitations of shared bus architectures. In real-time systems where bottlenecks can cause disastrous data loss, the inability to guarantee a sustainable throughput forces designers to significantly over-design solutions. The 64-bit and higher clock rate PCI solutions raise design expense and complexity and reduce the number of devices that can share the same bus. And still, the mighty bus arbiter has the final say in who gets the available resources.

In a point-to-point bus topology, a shared switch replaces the shared bus as the single shared resource by means of which all of the devices communicate (see Figure 2). Unlike in a shared bus topology, where the devices must collectively arbitrate among themselves for bus use, each device in the system has direct and exclusive access to the switch. In other words, each device sits on its own dedicated bus, which in PCI Express lingo is called a *link*.

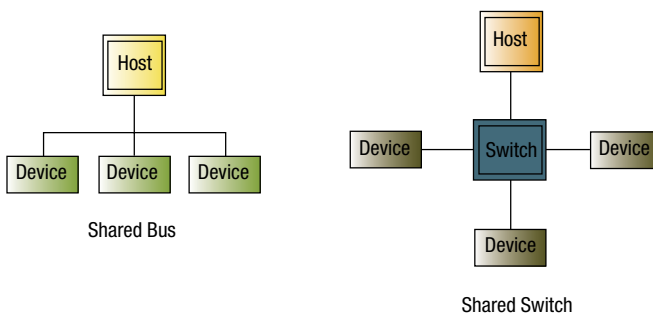


Figure 2

The emerging PCI Express standard now offers to provide a high-speed alternative by dedicating *lanes* for high-speed traffic within a computing environment. The concept involves establishing point-to-point, dedicated data lanes. The arbiter in the PCI world is replaced by a Root Complex that is designed to establish true point-to-point data links and then remove itself from the equation. The results are astounding with 4 GBps (16 lanes) in each direction with minimal overhead once the connection is established. PCI Express paves the way for superior performance in the most demanding real-time applications.

Real-world, real-time improvements

In real-time environments, PCI Express affords a clean pipeline for data with its point-to-point architecture. PCI Express also includes impressive expansion possibilities. With dedicated, uninterrupted high-speed bandwidth to each individual device on a dedicated lane and zero requirements for bridging, applications can extend over significant distances without suffering performance degradation. Systems with 150 I/O boards can be built, and additional

chassis can be connected with low-wire-count copper cabling that can operate at distances of up to seven meters.

The PCI Express specification will preserve software investments, and standard PCI and PCI Express cards can operate in the same system. Module manufacturers can supply instrument and I/O controllers that plug into PCI, PCI Express, or both buses. CompactPCI and PXI are also adopting the PCI Express specification to bring the same benefits to the industrial and test markets.

Solid-state drives reporting for duty

By Tom Bohman, VMETRO Inc.

Rotating storage fits many semi-rugged applications, but in platforms such as helicopters, tanks, and other tactical vehicles, hard disk drives usually can't survive for long once the action starts. This problem leaves these platforms' electronics designers with limited storage options.

For extremely harsh applications beyond the limits of hard disk drive technology, new solid-state drives are reporting for duty. Today's drives are denser, faster, more durable, and cost effective for use in a broader range of applications.

Ideally, packaging for these solid-state drives would allow them to fit next to existing electronics without requiring external boxes and additional connections. Since many tactical applications already have their electronics packaged in either conduction- or air-cooled ATR enclosures, one solution would be to mount the solid-state drives inside the ATR enclosure.

Designers could cobble together ad hoc solutions by mounting and cabling the drives. A more elegant solution, though, would mount solid-state drives on a carrier that inserts into an ATR slot the same way that signal processing and I/O hardware does. An example of this approach is the VMETRO VM-DRIVE (see figure), which mounts solid-state drives onto a carrier ready to fit into an available ATR slot.

With mounting accomplished, cabling is simplified. The carrier pulls the necessary power for the drives from either the VME or CompactPCI backplane in the ATR enclosure. Fibre Channel interfaces are designed into the unit and presented at the front panel. These can be cabled in various SAN topologies to high-performance dedi-

cated storage controllers or single board computers with Fibre Channel interfaces.

Solid-state drive solutions such as these give designers better options and simplify adding electronic storage to the most rugged tactical defense platforms.

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A single lane connecting two PCI Express termination devices is called a *by one* or written as an x1 link. More rapid interconnect speeds may be achieved by utilizing multiple lanes in parallel between PCI Express and termination devices such as sensors and recorders. Links can be increased from x1 to x16, which leads to performance ranges from 250 MBps to 4 GBps total bandwidth. In addition, all PCI Express lanes are full duplex, which allows data to flow in both directions simultaneously at full data rates.

At the top end, PCI Express can allow for performance up to 4 GBps for dedicated applications – first generation, 16 lanes, only counting one direction – or a 30x performance improvement over the base PCI implementation. That's four times faster than the fastest implementation of PCI Express (PCI-X 64/133). This allows an enormous opportunity for growth as PCI Express replaces shared bus architectures with its point-to-point functionality. PCI Express continues to capitalize on the high performance and low cost of PC technology that commodity desktop systems are shipping with PCI Express. As this first generation of PCI Express delivers much improved performance over PCI, PCI Express's next generation is being positioned to offer yet higher lane speeds. This will further break down traditional barriers to high-end data acquisition and recording.

The storm is here

PCI Express is highly scalable and takes advantage of newly available high-performance serial channels in FPGAs. These devices help bridge the development gap between legacy PCI buses and PCI Express. Hardware such as frame grabbers, controllers, and disk drives are able to easily capitalize on low-cost FPGAs to quickly implement PCI Express as we enter the petabyte (10^{15} bytes) world of massive storage potential.

Standard bus architectures including PCI, VME, PXI, and CompactPCI, in relative terms, have held data transfer rates in the slow zone. Shared bus arbitration has constrained the PCI bus, and high pin counts have made it too expensive and complex for wide adoption. Today, PCI Express offers an impressive theoretical threshold of 4 GBps top-end performance.

In addition to increased bus bandwidth advances, the disk drive industry has introduced advanced *perpendicular* – aligning the bits vertically, perpendicular to the disk to compress more data in less space – recording capability. By recording data vertically at densities of 230 GB/square inch, terabyte drives are now emerging. As data densities go up, data transfer rates also increase.

This will allow faster data recording for longer periods of time. Together with PCI Express, this advance in disk technology enables a new level of performance that was previously difficult and prohibitively expensive to attain.

PCI Express and other technology advances broaden the application set and enable Conduant and its StreamStor technology offerings to perform at full potential. Conduant's new PCI Express based product features four-lane endpoint connectivity to the host PCI Express fabric. Coupled with PCI Express, the full potential is limited only by the performance of the storage subsystems. With the introduction of PCI Express, data transfer rates have increased to 600 MBps (see Figure 3).

PCI Express

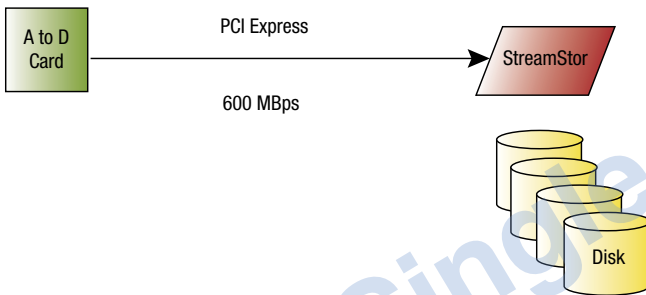


Figure 3

Lightning speeds usher in a new world of performance

Many industry segments are poised for the furious speeds PCI Express will make possible as components and peripherals are adapted to take advantage of the emerging technology. New applications will appear as the dedicated bandwidth of PCI Express allows the petabyte world to open up. As we see subsystems riding this emerging bus standard, new solutions and capabilities will unfold. The perfect storm is converging. ⚡



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Phil holds three U.S. patents relating to different methods of improving the performance of disk drives and systems. He earned his BSEE from the Rochester Institute of Technology.

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