Aerospace and defense programs drive some of the most challenging requirements. Long program lifetimes and stringent reliability add to complex trade-offs between performance, cost, and program schedule. Reconfigurable FPGAs are increasingly enabling these markets. Xilinx and other vendors provide long product life-cycle support as well as radiation-tolerant silicon and packaging. In addition, new FPGA capabilities such as embedded microprocessors and DSP are augmenting the reconfigurable FPGA’s inherent flexibility. One key design requirement revolves around high-assurance systems subject to atmospheric Neutron Single Event Upset (NSEU) radiation effects. A lack of consistent NSEU data combined with an abundance of opinions have clouded the true FPGA market requirement.

Experimentally measuring the NSEU sensitivity of any IC is a challenging task due to the low atmospheric neutron flux rates (even at elevated altitudes), the non-ideal flux-energy distributions found in highly accelerated neutron beam sources, and the small sample sizes available for testing. In addition, limited in-system test capability with some IC vendors makes data collection difficult or impossible. The designer requires NSEU data and an understanding of the system and environmental requirements in order to properly design an application to meet system reliability and availability specifications. The responsibility falls to the IC manufacturer to provide the designer the information required to properly evaluate a high-assurance system’s response to atmospheric radiation.

NSEU tolerance is not just an FPGA issue. State logic such as flip-flops and embedded memory in any generic IC is also susceptible to atmospheric radiation. While in many cases the IC state logic can be and often is more susceptible than an FPGA configuration memory cell, we will focus on the latter case only.

Xilinx has been studying NSEU and other radiation effects for a decade. It continues to perform extensive accelerated testing at the Los Alamos Neutron Science Center (LANSCE), as well as real-world NSEU testing at different altitudes and latitudes around the world. The latter test program is used to bridge the gap between accelerated testing and real-world results. After gathering and publishing thousands of device years’ worth of real-world test data, the conclusions are clear: Real-world testing is critical to demystifying NSEU effects, and reconfigurable FPGAs can meet the reliability targets demanded by the aerospace and defense market.

**NSEUs and NSEU data collection**

Atmospheric neutrons are residues of space – heavy ions – and solar particles like high-energy protons and coronal mass ejections, which impact the upper atmospheric nitrogen and oxygen atoms. These interactions create a collision cascade of particles, some of which are long lived and find their way down to the surface of the Earth. When they reach Earth, this cascade of particles is composed primarily of high-energy neutrons plus a small altitude-dependent percentage of protons (Figure 1). These neutrons will interact with matter. A neutron interacting with a silicon nucleus can create alpha particles and other charged nuclei that create a charge tail.

- High-energy (>> GeV) primary particles from the cosmos don’t make it to terrestrial levels (~0 to 10 kFT)
- High energy neutrons:
  - Make it through the atmosphere to terrestrial levels in significant numbers
  - Can penetrate semiconductor packaging
  - Have some finite scattering cross section (that is, can cause upset)

![Schematic Diagram of Cosmic Ray Shower](image)

**Figure 1**
If strong enough, the charge tail may flip a bit or change state in an SRAM memory, a latch, or FPGA configuration cell. This upset is called an NSEU or soft error, since no permanent damage is done to the latch. Depending on the function being performed, the NSEU may affect the functional output of the device in the case of an upset configuration cell (Figure 2).

A seemingly trivial question is: What is the total neutron flux and flux rate that an FPGA designer must account for when designing a system to meet specific customer requirements? In a study of studies on the experimental measurement of neutron flux and energy, Ziegler[1] showed that previous results varied widely and can lead to errors of as much as 10 to 1 in neutron flux and/or neutron energy profiles at any specific site, depending on the data set chosen (Figure 3). With a 10 to 1 error, you could basically pick any answer you wanted.

This wide range of data introduces uncertainty in the neutron flux and/or neutron energy that must be accounted for in the design effort. The engineering team ultimately will be held accountable for the long-term success of their program and can’t afford to design to speculation. Rather, they must design to meet hard system reliability and availability specifications, as well as to support their design choices with reliable, accurate neutron sensitivity data.

IC soft errors are primarily caused by neutron-induced SEUs

Understanding the necessary terminology

When further delving into the details of neutron single-event phenomena in FPGAs, it’s important to first understand some basic definitions. They are:

- **Soft error**: An NSEU-induced bit-flip in the configuration memory. Soft errors may or may not induce a functional error and are correctable with no permanent damage to the cell, hence the term soft.

- **User Logic Upset Rate (functional failure)**: Incorrect design behavior caused by a soft error in a critical configuration memory cell.

- **SEU Probability Index (SEUPI)**: The ratio between the soft error rate and the functional failure rate. In Xilinx devices, for example, the SEUPI value is conservatively estimated at 10:1. This means that a designer can expect one functional failure for every 10 soft errors.

- **Single Event Functional Interrupt (SEFI)**: A functional error that requires FPGA reconfiguration or power cycle to erase the error.

It should be noted that soft errors and SEFIs are often mixed up in literature. In fact, soft errors are not equivalent to SEFIs, or even to logic upsets.
Accelerated neutron beam testing of FPGAs is one useful way to approximate reality. An example is the neutron beam at the Los Alamos Neutron Science Center. Its beam profile is a reasonable fit to theoretical atmospheric neutron profiles, but at much higher flux. This higher flux enables much faster testing than a real-world test, which would require multiple years or large numbers of devices (Figure 4).

While accelerated neutron beam testing may point the engineering team in the right direction, correlating those accelerated testing results to real-world performance of hundreds of parts over many months or years, at multiple locations (altitudes and latitudes), is required. In addition, accelerated testing typically involves exposing at least a few devices to an artifact (the beam) that simulates and accelerates, but which does not really recreate the natural environment. Another drawback is that the beam is just a reasonable fit – off by 3x at lower energies (refer to Figure 4). Also, experimental results can vary over each run; we have seen variations up to ± 20 percent.

Real-world data
To account for these variations, Xilinx embarked on a program called Rosetta [2] four years ago that measures real-world NSEU effects in FPGAs. Hundreds of devices are being monitored for NSEU effects at several diverse atmospheric locations such as Albuquerque, New Mexico (5,100 feet), San Jose, California (0 feet altitude), White Mountain, California (12,500 feet), Toulouse, France (472 feet), Plateau de Bare, France (8,171 feet), Mauna Kea, Hawaii (13,200 feet), and in a nuclear storage bunker 1,500 feet below ground level in Toulouse, France. Figures 5 and 6 show the inside and outside of the White Mountain facility.

In total, Rosetta has obtained more than 220,000 Mbit-years’ worth of testing over multiple process geometries. Further testing is ongoing. An Mbit-year is defined as 1 Mbit worth of configuration data testing over the span of one year. Xilinx realized 1,700 device hours of testing in the LANSCE beam last year alone. Multiplied by the acceleration factor of 10^5 (the factor of beam neutrons over normal sea-level atmospheric neutrons), this corresponds to 335,000 Mbit-years of beam testing. This amount of testing is orders of magnitude more than typical program lifetimes.

Neutron exposures are performed at the ICE house (Integrated Circuit Exposure facility) where a neutron beam with an energy distribution similar to the atmospheric neutron flux at 40,000 ft is available.

Comparison of Neutron Spectra

![Figure 4](image-url)
The results of both test methods are detailed in Table 1. Note that both FPGA configuration bit upsets and any Single Event Functional Interrupts (SEFIs) were monitored. To date, no SEFIs have occurred in the Rosetta testing. The cross-section is the altitude independent, normalized measure of device NSEU susceptibility.

Converting the cross-section to Failure in Time (FIT)/Mb can be accomplished via the following equation: \( \text{FIT/Mb} = \text{Cross-section} \times 14.4 \times 10^9 \times 10^6 \), where \( 10^9 \) is the FIT definition (1 FIT is per billion hours), \( 10^6 \) is to normalize per Mbit (\( 10^6 \) bits) of configuration data, and 14.4 is the sea level neutron flux per square centimeter-hr.

The data is striking. One would assume that shrinking IC process geometries would imply worsening NSEU tolerance, as is feared – and has been actually seen – in some commercial SRAMs. The charge storage at a 90-nm gate is smaller than at 130 nm, meaning there should be less charge (created by a neutron spallation reactions) required to upset those bits. Yet the shrinking cross-section and lower failure in time or FIT rate show otherwise. Note that NSEU tolerance in Xilinx designs also has improved for new designs within each process node over time since the 220 nm node.

The high-performance, feature-rich FPGA configuration cells that Xilinx uses are sometimes confused with simple SRAMs. Xilinx designs its static-latch configuration cell to a different standard than SRAMs. This data shows that the static-latch design has not only stabilized but improved both over earlier process nodes as well as within process nodes. Xilinx also designs its lookup table logic to the same standards of reliability.

Based on the results of this testing, Xilinx correlated the real world to the accelerated testing data sets of its products. It determined the correct neutron energy model (>10 MeV) that correlates with the real world to use when calculating upset rates using accelerated testing data. Based on this corrected energy model, it was determined that FPGAs in the real world are less susceptible to NSEU effects than predicted by accelerated testing by around a factor of up to 5 times, especially at smaller process nodes. Note, therefore, it is incorrect to extrapolate the 1.5-MeV model, which is often used in SRAM data calculations and many FPGA procurement specifications.

Real-world data now enables faster time to evaluate FPGA designs in an accelerated beam, more accurately correlating accelerated beam data to what can be expected in the real world. These experiments also show the importance of Rosetta-like experiments for any accelerated tests on an FPGA or an IC such as an ASIC.

Is the NSEU a functional error? The SEU Probability Index (SEUPI) is the ratio between configuration bit upsets and functional failures (user logic upsets). Many Xilinx customers have performed their own studies and shown that the ratio
of NSEUs to logic upsets can be as high as 25 to 100 times. Stated differently, an accumulation of 25 to 100 configuration cell soft errors is typically required to cause a functional failure. A conservative rule of thumb is that since at most ~10 percent of the configuration cells – even in a dense design – are used in a typical FPGA design, the ratio of soft errors to logic upsets is at least 10 to 1. The logic upset rate of an FPGA is very small compared to the configuration cell upset rate.

True upset rates can now be calculated to show the insensitivity of static-latch FPGAs to NSEUs. As previously mentioned, cross-section is defined as the common measure of NSEU upset rates – the probability that a single neutron flips a single bit. Given that, Mean Time to Functional Failure (MTTFF) can be calculated as follows:

\[
\text{Sea Level MTTFF (hours)} = \frac{\text{SEUPI}}{[1/(\text{Configuration Bits}*\text{Neutron Cross Section})*14.4]}
\]

or

\[
\text{Sea Level MTTFF (hours)} = \frac{\text{SEUPI}}{[10^7/(\text{Mb of Configuration Bits}*\text{FIT/Mb rate})]}
\]

Hours can then be converted to years by the standard 24 hours/day * 365 days/year factor. In Table 2, altitude multiplying (reduction) factors are calculated using the JEDEC standard number JESD89 above the Sea Level value of 14.4 (a 9.73 reduction factor at 10,000 feet).

Note that while the largest, most dense Virtex-4 devices can have on the order of 51 Mbits of configuration data, the factor of a 3.5 reduction is still a large MTTFF. There are also factors such as latitude and even sunspots that add some additional bound on these numbers; both those effects aren’t large enough in aggregate to impact these conclusions. In fact, the table is conservative given the low choice of the SEUPI factor of 10.

### Real-world results are the key

Although there will always be application-dependant choices in design, a couple of threads are common to these design problems in achieving NSEU tolerance. First, it is critical to use the correct neutron models. Second, while accelerated testing helps shorten the time it takes to evaluate NSEU effects, this testing must be correlated to real-world results to ensure that accurate requirements are obtained.

Xilinx has invested more than 230,000 Mbit-years of real-world testing in dealing with the issue of neutron single-event phenomena. More importantly, it has taken the known unknown of NSEUs and quantified it, enabling designers to use reasonable design margins to reach their reliability targets. Armed with this information, reconfigurable FPGAs can be confidently used over less capable technologies.

### Table 2

<table>
<thead>
<tr>
<th>Device</th>
<th>Altitude</th>
<th>Config. memory size</th>
<th>Rosetta Configuration bit FIT rate (FIT/Mb)</th>
<th>MTTFF including SEUPI correction of 10</th>
</tr>
</thead>
<tbody>
<tr>
<td>4VLX25</td>
<td>0 feet</td>
<td>8 MBit</td>
<td>48</td>
<td>3,000 years</td>
</tr>
<tr>
<td>4VLX25</td>
<td>10,000 feet</td>
<td>8 MBit</td>
<td>48</td>
<td>310 years</td>
</tr>
<tr>
<td>4VSX35</td>
<td>0 feet</td>
<td>14.5 MBit</td>
<td>48</td>
<td>1,650 years</td>
</tr>
<tr>
<td>4VSX35</td>
<td>10,000 feet</td>
<td>14.5 MBit</td>
<td>48</td>
<td>170 years</td>
</tr>
</tbody>
</table>

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References


Editor's note: Since this article was written, Xilinx has released the Spartan-3A (S3A) platform (in a 90 nm process) and the Virtex-5 (V5) platform (in a 65 nm process). In both cases, preliminary NSEU data shows improvement over previously released 90 nm products and improvement at the 65 nm process node, which further supports the thesis of this article. Contact Xilinx directly for more information.